In The Claims:

Claim 1. (currently amended) A split-gate non-volatile memory cell, comprising:

a substrate;

a charge-trapping layer on the substrate;

a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer, wherein the split gate is composed of at least two separated conductive pieces and the conductive pieces are electrically connected to a common voltage source; and

a source/drain in the substrate beside the split gate, wherein

the charge-trapping layer around the split region serves as a coding region.

Claim 2-3 (canceled)

Claim 4. (currently amended) The split-gate non-volatile memory cell of claim ~~3~~ 1, wherein the ~~three~~ conductive pieces of the split gate include a pair of conductive spacers and a conductive layer between the pair of conductive spacers.

Claim 5. (original) The split-gate non-volatile memory cell of claim 4, wherein the pair of conductive spacers are arranged with two substantially vertical sidewalls thereof adjacent to the source/drain.

Claim 6. (original) The split-gate non-volatile memory cell of claim 5, further comprising an insulator on the source/drain, wherein the pair of conductive spacers are disposed on the sidewalls of the insulator.

Claim 7 (canceled)

Claim 8. (currently amended) The split-gate non-volatile memory cell of claim ~~2~~ 1, wherein the conductive pieces are separated from each other by a dielectric layer ~~comprises silicon oxide~~.

Claim 9. (original) The split-gate non-volatile memory cell of claim 1, wherein the split gate comprises polysilicon.

Claim 10. (original) The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises a silicon nitride layer disposed between two silicon oxide layers.

Claim 11. (original) The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises aluminum oxide (Al2O3).

Claim 12. (original) The split-gate non-volatile memory cell of claim 1, wherein the substrate comprises a p-substrate, and the source/drain comprises an n-type source/drain.

Claims 13-34 (canceled)

Claim 35. (currently amended) An operating method of a split-gate non-volatile memory cell, wherein

the split-gate non-volatile memory cell comprises:

a substrate;

a charge-trapping layer on the substrate;

a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer, wherein the charge-trapping layer around the split region

serves as a coding region, the split gate is composed of at least two separated conductive pieces and the conductive pieces are electrically connected to a common voltage source; and

a source/drain in the substrate beside the split gate, and

the operating method comprises:

in a programming operation:

applying 0V to the substrate and the source/drain; and

applying a first negative voltage to the split gate, the first negative voltage being sufficiently high for injecting electrons into the coding region; and

in an erasing operation:

applying 0V to the split gate, wherein each conductive piece is at an electric state of 0 V;

floating the source/drain; and

applying a second negative voltage to the substrate, the second positive voltage being sufficiently high for ejecting electrons from the coding region.

Claim 36. (original) The operating method of claim 35, wherein the first negative voltage is about –10V.

Claim 37. (original) The operating method of claim 35, wherein the second negative voltage is about –10V.

Claims 38-45 (canceled)